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ALIGNAB	7
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ALIGNABE	3
ALIGNABEL	1
ALIGNABIC	1
ALIGNABIE	24
ALIGNABILE	1
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L16

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DATE: Tuesday, March 16, 2004 [Printable Copy](#) [Create Case](#)

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DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

<u>L16</u>	L15 and align\$7	51	<u>L16</u>
<u>L15</u>	L14 and l4	67	<u>L15</u>
<u>L14</u>	L13 and (simd or single near1 instruction near2 multiple)	67	<u>L14</u>
<u>L13</u>	L12 and l4	124	<u>L13</u>
<u>L12</u>	L11 and vector\$1 near3 register\$1	155	<u>L12</u>
<u>L11</u>	(result\$3 or combin\$6 or insert\$3 or integrat\$3 or mix\$3) near5 vector\$1 and L9	201	<u>L11</u>
<u>L10</u>	l4 and L9	176	<u>L10</u>
<u>L9</u>	L7 and (simd or single near1 instruction)	262	<u>L9</u>
<u>L8</u>	L7 and l1	0	<u>L8</u>
<u>L7</u>	(shift\$3 or concatenat\$3) near5 vector\$1	6606	<u>L7</u>
<u>L6</u>	l4 and l5	43	<u>L6</u>
<u>L5</u>	L2 and vector\$1 near5 register\$1 and (result\$3 or combin\$6 or insert\$3 or integrat\$3 or mix\$3) near5 vector\$1	57	<u>L5</u>

DB=PGPB,USPT; PLUR=YES; OP=OR

<u>L4</u>	(712/2-300)![CCLS]	9541	<u>L4</u>
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DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

<u>L3</u>	L2 and vector\$1 near5 register\$1	65	<u>L3</u>
<u>L2</u>	(simd or single near1 instruction) and align\$7 near4 vector\$1	84	<u>L2</u>
<u>L1</u>	(simd or single near1 instruction) and aling\$7 near4 vector\$1	0	<u>L1</u>

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Search Results - Record(s) 1 through 20 of 67 returned.

☐ 1. Document ID: US 20040044882 A1

Using default format because multiple data bases are involved.

L15: Entry 1 of 67

File: PGPB

Mar 4, 2004

PGPUB-DOCUMENT-NUMBER: 20040044882

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040044882 A1

TITLE: selective bypassing of a multi-port register file

PUBLICATION-DATE: March 4, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Asaad, Sameh	Briarcliff Manor	NY	US	
Moreno, Jaime H.	Dobbs Ferry	NY	US	
Zyuban, Victor	Yorktown Heights	NY	US	

US-CL-CURRENT: 712/218

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Drawings
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☐ 2. Document ID: US 20040030863 A1

L15: Entry 2 of 67

File: PGPB

Feb 12, 2004

PGPUB-DOCUMENT-NUMBER: 20040030863

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040030863 A1

TITLE: Multimedia coprocessor control mechanism including alignment or broadcast instructions

PUBLICATION-DATE: February 12, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Paver, Nigel C.	Austin	TX	US	
Yu, Wing K.	Chandler	AZ	US	
Ganeshan, Murli	Austin	TX	US	

US-CL-CURRENT: 712/34

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw. De
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☐ 3. Document ID: US 20040030862 A1

L15: Entry 3 of 67

File: PGPB

Feb 12, 2004

PGPUB-DOCUMENT-NUMBER: 20040030862

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040030862 A1

TITLE: Multimedia coprocessor control mechanism

PUBLICATION-DATE: February 12, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Paver, Nigel C.	Austin	TX	US	
Maghielse, William T.	Austin	TX	US	
Yu, Wing K.	Chandler	AZ	US	
Liu, Jianwei	Austin	TX	US	
Jebson, Anthony	Austin	TX	US	
Bavaria, Kailesh B.	Austin	TX	US	
Parikh, Rupal M.	Austin	TX	US	
Deng, Deli	Austin	TX	US	
Patel, Mukesh	Austin	TX	US	
Fullerton, Mark	Austin	TX	US	
Ganeshan, Murli	Austin	TX	US	
Strazdus, Stephen J.	Chandler	AZ	US	

US-CL-CURRENT: 712/34; 712/210

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw. De
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☐ 4. Document ID: US 20040006681 A1

L15: Entry 4 of 67

File: PGPB

Jan 8, 2004

PGPUB-DOCUMENT-NUMBER: 20040006681

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040006681 A1

TITLE: Viterbi decoding for SIMD vector processors with indirect vector element access

PUBLICATION-DATE: January 8, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
------	------	-------	---------	---------

h e b b g e e e f e f e f b e

Moreno, Jaime Humberto	Dobbs Ferry	NY	US
Neaser, Fredy Daniel	Langnau am Albis		CH

US-CL-CURRENT: 712/4

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMIC	Draw D
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☐ 5. Document ID: US 20030037221 A1

L15: Entry 5 of 67

File: PGPB

Feb 20, 2003

PGPUB-DOCUMENT-NUMBER: 20030037221
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030037221 A1

TITLE: Processor implementation having unified scalar and SIMD datapath

PUBLICATION-DATE: February 20, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Gschwind, Michael Karl	Mohegan Lake	NY	US	
Hofstee, Harm Peter	Austin	TX	US	
Hopkins, Martin Edward	Chappaqua	NY	US	

US-CL-CURRENT: 712/3; 712/222, 712/229, 712/43, 712/7

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMIC	Draw D
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☐ 6. Document ID: US 20020116595 A1

L15: Entry 6 of 67

File: PGPB

Aug 22, 2002

PGPUB-DOCUMENT-NUMBER: 20020116595
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020116595 A1

TITLE: Digital signal processor integrated circuit

PUBLICATION-DATE: August 22, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Morton, Steven G.	Oxford	CT	US	

US-CL-CURRENT: 712/22

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMIC	Draw D
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☐ 7. Document ID: US 20020062436 A1

L15: Entry 7 of 67

File: PGPB

May 23, 2002

PGPUB-DOCUMENT-NUMBER: 20020062436

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020062436 A1

TITLE: METHOD FOR PROVIDING EXTENDED PRECISION IN SIMD VECTOR ARITHMETIC OPERATIONS

PUBLICATION-DATE: May 23, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
VAN HOOK, TIMOTHY J.	VAN HOOK	CA	US	
HSU, PETER	FREMONT	CA	US	
HUFFMAN, WILLIAM A.	LOS GATOS	CA	US	
MORETON, HENRY P.	WOODSIDE	CA	US	
KILLIAN, EARL A.	LOS ALTOS HILLS	CA	US	

US-CL-CURRENT: 712/210; 712/222

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 8. Document ID: US 6665790 B1

L15: Entry 8 of 67

File: USPT

Dec 16, 2003

US-PAT-NO: 6665790

DOCUMENT-IDENTIFIER: US 6665790 B1

TITLE: Vector register file with arbitrary vector addressing

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 9. Document ID: US 6647485 B2

L15: Entry 9 of 67

File: USPT

Nov 11, 2003

US-PAT-NO: 6647485

DOCUMENT-IDENTIFIER: US 6647485 B2

TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 10. Document ID: US 6334176 B1

L15: Entry 10 of 67

File: USPT

Dec 25, 2001

US-PAT-NO: 6334176

DOCUMENT-IDENTIFIER: US 6334176 B1

TITLE: Method and apparatus for generating an alignment control vector

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 11. Document ID: US 6321327 B1

L15: Entry 11 of 67

File: USPT

Nov 20, 2001

US-PAT-NO: 6321327

DOCUMENT-IDENTIFIER: US 6321327 B1

TITLE: Method for setting a bit associated with each component of packed floating-point operand that is normalized in SIMD operations

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 12. Document ID: US 6317819 B1

L15: Entry 12 of 67

File: USPT

Nov 13, 2001

US-PAT-NO: 6317819

DOCUMENT-IDENTIFIER: US 6317819 B1

TITLE: Digital signal processor containing scalar processor and a plurality of vector processors operating from a single instruction

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 13. Document ID: US 6292886 B1

L15: Entry 13 of 67

File: USPT

Sep 18, 2001

US-PAT-NO: 6292886

DOCUMENT-IDENTIFIER: US 6292886 B1

TITLE: Scalar hardware for performing SIMD operations

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 14. Document ID: US 6282630 B1

L15: Entry 14 of 67

File: USPT

Aug 28, 2001

US-PAT-NO: 6282630

DOCUMENT-IDENTIFIER: US 6282630 B1

TITLE: High-performance, superscalar-based computer system with out-of-order

instruction execution and concurrent results distribution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 15. Document ID: US 6272619 B1

L15: Entry 15 of 67

File: USPT

Aug 7, 2001

US-PAT-NO: 6272619

DOCUMENT-IDENTIFIER: US 6272619 B1

TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 16. Document ID: US 6266758 B1

L15: Entry 16 of 67

File: USPT

Jul 24, 2001

US-PAT-NO: 6266758

DOCUMENT-IDENTIFIER: US 6266758 B1

TITLE: Alignment and ordering of vector elements for single instruction multiple data processing

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 17. Document ID: US 6256720 B1

L15: Entry 17 of 67

File: USPT

Jul 3, 2001

US-PAT-NO: 6256720

DOCUMENT-IDENTIFIER: US 6256720 B1

TITLE: High performance, superscalar-based computer system with out-of-order instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 18. Document ID: US 6219775 B1

L15: Entry 18 of 67

File: USPT

Apr 17, 2001

US-PAT-NO: 6219775

DOCUMENT-IDENTIFIER: US 6219775 B1

TITLE: Massively parallel computer including auxiliary vector processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMMC	Draw. Des
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☐ 19. Document ID: US 6212619 B1

L15: Entry 19 of 67

File: USPT

Apr 3, 2001

US-PAT-NO: 6212619

DOCUMENT-IDENTIFIER: US 6212619 B1

**** See image for Certificate of Correction ****

TITLE: System and method for high-speed register renaming by counting

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMMC	Draw. Des
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☐ 20. Document ID: US 6128723 A

L15: Entry 20 of 67

File: USPT

Oct 3, 2000

US-PAT-NO: 6128723

DOCUMENT-IDENTIFIER: US 6128723 A

TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMMC	Draw. Des
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Term	Documents
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(L14 AND L4).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	67

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☐ 21. Document ID: US 6101594 A

Using default format because multiple data bases are involved.

L15: Entry 21 of 67

File: USPT

Aug 8, 2000

US-PAT-NO: 6101594

DOCUMENT-IDENTIFIER: US 6101594 A

TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

DATE-ISSUED: August 8, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nguyen; Le Trong	Monte Sereno	CA		
Lentz; Derek J.	Los Gatos	CA		
Miyayama; Yoshiyuki	Santa Clara	CA		
Garg; Sanjiv	Freemont	CA		
Hagiwara; Yasuaki	Santa Clara	CA		
Wang; Johannes	Redwood City	CA		
Lau; Te-Li	Palo Alto	CA		
Wang; Sze-Shun	San Diego	CA		
Trang; Quang H.	San Jose	CA		

US-CL-CURRENT: 712/41; 712/206, 712/215, 712/23, 712/245, 712/42

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 22. Document ID: US 6098162 A

L15: Entry 22 of 67

File: USPT

Aug 1, 2000

US-PAT-NO: 6098162

DOCUMENT-IDENTIFIER: US 6098162 A

TITLE: Vector shift functional unit for successively shifting operands stored in a vector register by corresponding shift counts stored in another vector register

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 23. Document ID: US 6092181 A

L15: Entry 23 of 67

File: USPT

Jul 18, 2000

US-PAT-NO: 6092181

DOCUMENT-IDENTIFIER: US 6092181 A

**** See image for Certificate of Correction ****

TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw De
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☐ 24. Document ID: US 6088783 A

L15: Entry 24 of 67

File: USPT

Jul 11, 2000

US-PAT-NO: 6088783

DOCUMENT-IDENTIFIER: US 6088783 A

TITLE: DPS having a plurality of like processors controlled in parallel by an instruction word, and a control processor also controlled by the instruction word

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw De
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☐ 25. Document ID: US 6088782 A

L15: Entry 25 of 67

File: USPT

Jul 11, 2000

US-PAT-NO: 6088782

DOCUMENT-IDENTIFIER: US 6088782 A

TITLE: Method and apparatus for moving data in a parallel processor using source and destination vector registers

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw De
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☐ 26. Document ID: US 6085275 A

L15: Entry 26 of 67

File: USPT

Jul 4, 2000

US-PAT-NO: 6085275

DOCUMENT-IDENTIFIER: US 6085275 A

**** See image for Certificate of Correction ****

TITLE: Data processing system and method thereof

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw De
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☐ 27. Document ID: US 6061521 A

L15: Entry 27 of 67

File: USPT

May 9, 2000

US-PAT-NO: 6061521

DOCUMENT-IDENTIFIER: US 6061521 A

TITLE: Computer having multimedia operations executable as two distinct sets of operations within a single instruction cycle

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw De
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☐ 28. Document ID: US 6038654 A

L15: Entry 28 of 67

File: USPT

Mar 14, 2000

US-PAT-NO: 6038654

DOCUMENT-IDENTIFIER: US 6038654 A

**** See image for Certificate of Correction ****

TITLE: High performance, superscalar-based computer system with out-of-order instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw De
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☐ 29. Document ID: US 6038653 A

L15: Entry 29 of 67

File: USPT

Mar 14, 2000

US-PAT-NO: 6038653

DOCUMENT-IDENTIFIER: US 6038653 A

**** See image for Certificate of Correction ****

TITLE: High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw De
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☐ 30. Document ID: US 5996057 A

L15: Entry 30 of 67

File: USPT

Nov 30, 1999

US-PAT-NO: 5996057

DOCUMENT-IDENTIFIER: US 5996057 A

TITLE: Data processing system and method of permutation with replication within a vector register file

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw De
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☐ 31. Document ID: US 5961629 A

L15: Entry 31 of 67

File: USPT

Oct 5, 1999

US-PAT-NO: 5961629

DOCUMENT-IDENTIFIER: US 5961629 A

TITLE: High performance, superscalar-based computer system with out-of-order instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 32. Document ID: US 5933650 A

L15: Entry 32 of 67

File: USPT

Aug 3, 1999

US-PAT-NO: 5933650

DOCUMENT-IDENTIFIER: US 5933650 A

TITLE: Alignment and ordering of vector elements for single instruction multiple data processing

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 33. Document ID: US 5922066 A

L15: Entry 33 of 67

File: USPT

Jul 13, 1999

US-PAT-NO: 5922066

DOCUMENT-IDENTIFIER: US 5922066 A

TITLE: Multifunction data aligner in wide data width processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 34. Document ID: US 5887183 A

L15: Entry 34 of 67

File: USPT

Mar 23, 1999

US-PAT-NO: 5887183

DOCUMENT-IDENTIFIER: US 5887183 A

**** See image for Certificate of Correction ****

TITLE: Method and system in a data processing system for loading and storing vectors in a plurality of modes

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 35. Document ID: US 5875315 A

L15: Entry 35 of 67

File: USPT

Feb 23, 1999

US-PAT-NO: 5875315

DOCUMENT-IDENTIFIER: US 5875315 A

**** See image for Certificate of Correction ****

TITLE: Parallel and scalable instruction scanning unit

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 36. Document ID: US 5872987 A

L15: Entry 36 of 67

File: USPT

Feb 16, 1999

US-PAT-NO: 5872987

DOCUMENT-IDENTIFIER: US 5872987 A

TITLE: Massively parallel computer including auxiliary vector processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 37. Document ID: US 5867683 A

L15: Entry 37 of 67

File: USPT

Feb 2, 1999

US-PAT-NO: 5867683

DOCUMENT-IDENTIFIER: US 5867683 A

**** See image for Certificate of Correction ****

TITLE: Method of operating a high performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating point operations

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 38. Document ID: US 5867682 A

L15: Entry 38 of 67

File: USPT

Feb 2, 1999

US-PAT-NO: 5867682

DOCUMENT-IDENTIFIER: US 5867682 A

TITLE: High performance superscalar microprocessor including a circuit for converting CISC instructions to RISC operations

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 39. Document ID: US 5864703 A

L15: Entry 39 of 67

File: USPT

Jan 26, 1999

US-PAT-NO: 5864703

DOCUMENT-IDENTIFIER: US 5864703 A

TITLE: Method for providing extended precision in SIMD vector arithmetic operations

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 40. Document ID: US 5860085 A

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TITLE: Instruction set for a content addressable memory array with read/write circuits and an interface register logic block

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